

Notice of References Cited	Application/Control No. 10/040,953	Applicant(s)/Patent Under Reexamination TEIG ET AL.	
	Examiner Andrea Liu	Art Unit 2825	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
*	U	Resolving horizontal constraints and minimizing net wire length for multi-layer channel routing Pal, R.K.; Datta, A.K.; Pal, S.P.; Pal, A.; TENCON '93. Proceedings. Computer, Communication, Control and Power Engineering. 1993 IEEE Region 10 Conference
*	V	Hierarchical physical design system Schulz, U., CompEuro '89., 'VLSI and Computer Peripherals. VLSI and Microelectronic Applications in Intelligent Peripherals and their Interconnection Networks', Proceedings., 8-12 May 1989
*	W	On the integration of partitioning and global routing for rectilinear placement problems Chingwei Yeh; Chi-Shong Wang; Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 15 , Issue: 1 , Jan. 1996
*	X	Timing-driven hierarchical global routing with wire-sizing and buffer-insertion for VLSI with multi-routing-layer Deguchi, T.; Koide, T.; Wakabayashi, S.; Design Automation Conference, 2000. Proceedings of the ASP-DAC 2000. Asia and South Pacific , 25-28

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Notice of References Cited	Application/Control No. 10/040,953	Applicant(s)/Patent Under Reexamination TEIG ET AL.	
	Examiner Andrea Liu	Art Unit 2825	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
X	U	Resolving horizontal constraints and minimizing net wire length for multi-layer channel routing Pal, R.K.; Datta, A.K.; Pal, S.P.; Pal, A.; TENCON '93. Proceedings. Computer, Communication, Control and Power Engineering. 1993 IEEE Region 10 Conference
X	V	Hierarchical physical design system Schulz, U.; CompEuro '89., 'VLSI and Computer Peripherals. VLSI and Microelectronic Applications in Intelligent Peripherals and their Interconnection Networks', Proceedings. , 8-12 May 1989
X	W	On the integration of partitioning and global routing for rectilinear placement problems Chingwei Yeh; Chi-Shong Wang; Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 15 , Issue: 1 , Jan. 1996
X	X	Timing-driven hierarchical global routing with wire-sizing and buffer-insertion for VLSI with multi-routing-layer Deguchi, T.; Koide, T.; Wakabayashi, S.; Design Automation Conference, 2000. Proceedings of the ASP-DAC 2000. Asia and South Pacific , 25-28

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.